UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,627	11/20/2001	Glen Hush	M4065.0478/P478	8791

24998 7590 05/30/2003

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER	
NGUYEN, NAM THANH	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 05/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,627	HUSH ET AL.	
	Examiner	Art Unit	
	Nam t Nguyen	2824	

-- Th MAILING DATE of this communication appears on the cov r sh et with the correspond nce addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2002 (the amendment A)* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: *east search history* .

DETAILED ACTION

1. The amendment A filed on 2/12/03 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1-27, 42-58 are rejected under 35 U.S.C. 102(e) as being anticipated by Loerey et al (U.S. Patent No 6,314,014).

With respect to claims 1, 14, 27, figure 2a of Lowrey discloses a memory device comprising a first digit line (CL4) and a second digit line (CL5), a first programmable conductor memory element (120), a second programmable conductor memory element (130), a first access device (the transistor that connected between the first programmable conductor memory element 120 and the first digit line CL4), a second access device (the transistor that connected between the programmable memory element 130 and the second digit line CL5), and a sense amplifier (SA4) having inputs coupled to the first digit line CL4 and the second digit line CL5.

Regarding claims 2, 15, figure 6B of Lowrey et al teaches a precharge circuit (VPRE) for precharging the first and second digit lines (551, 552) to a precharge voltage prior the read operation. See column 10, lines 44-60 of Lowrey et al.

Regarding claims 53 and 59, the method of forming first and second digit lines, first and second programmable conductor memory elements, first and second access transistors, a precharge circuit and a sense amplifier are disclosed in Lowrey et al as set forth in the rejection of claims 1, 14 and 27 above. Further, the circuit for operating the access transistor (in claim 59) is inherently included in Lowrey et al since every memory device must have a row address decoder connected to the word line so as to operate the access transistor (select an address in a memory device).

As of claims 3, 16 and 54, figure 2 A of Lowrey et al discloses a pair of row lines (or word lines) which connected to the access device (or access transistor, the transistor that connected between row lines and the memory element. In addition, since every memory device must have a row decoder connected to the row lines (or word lines) so as to select the word lines or row lines, then the reference of Lowrey et al inherently includes a row decoder as claimed in claim 54. Also, the first and second digit lines in Lowrey et al are selected at the same time (namely CL4 and CL5), then the decoder used in Lowrey et al clearly activating the first and the second row lines simultaneously.

Regarding claims 4, 17, the access device (Q1, figure 2A) is an access transistor.

With respect to claims 5, 18 and 55, column 22, lines 13-29, clearly teaches that the first and second programmable conductor elements 120 and 130 are made of a phase change material which is chalcogenide.

With respect to claims 6 and 19, when the access transistor Q1 is on, the precharge voltage at the digit lines CL4 and CL5 would be discharge through the programmable conductor memory element.

Regarding claims 7-8 and 20-21, column 11, lines 20-45 of Lowrey et al teaches that the digit lines CL4 and CL5 have an associated parasitic capacitance, and the voltage value of such parasitic capacitance is higher the VPRE.

With respect to claims 9-10 and 22-23, when the row line RL1 is on, the access transistor is on, then the memory element is automatically refresh. When the row line RL1 is deactivated, the access transistor Q1 is off, then the refresh operation is prevented

As of claims 11-12, 24-25 and 56-57, figure 2A of Lowrey et al shows that the first cell 120 and the second cell (the cell that connected between RL1 and CL5) are in a common memory array, and figure 6C shows that the first cell 120 and the second cell (131B) are in a different memory arrays.

Regarding claims 13, 26, 58, figure 6B of Lowrey et al discloses an equalizer (Q21 and /Q22) for equalizing the digit lines 552.

With respect to claims 42 - 44 , the step of storing data is performed by the memory element M (fig.2A), the step of determining the resistance of the memory

element is performed by sense amplifier SA4 and the steps of prechaging and discharging are performed by VPRE (fig. 6B) and access transistor Q1.

As of claims 45 and 46, since the precharge voltage VPRE is cut off before the access transistor is on and the Q21 (fig. 6B) is cur off before the selection of the access transistor, then precharge cycle is completed before enabling the access transistor.

With respect to claims 47 –49 and 51-52, the comparison circuit (or sense amplifier) in Lowrey et al would perform the function of determining the discharge voltage associated with the memory element, and set the digit lines which has a higher discharge voltage to a first voltage state and set the digit lines which has a lower discharge voltage to a second voltage state. See column 19 lines 64-66 and column 20, lines 1-65. .

With respect to claim 50, column 8, lines 60-65 teaches that the second voltage is ground voltage.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 28, 29-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lowrey et al.

The only difference between Lowrey et al and claims 29-41 is that Lowrey et al is silent on the use of a microprocessor connected to their memory device in order to control the operation (read, write) of the memory device. However, it is well known in the memory art that every memory system must have a microprocessor connected the storage device so as to control the operation to the storage device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lowrey et al by using a microprocessor coupled to the storage device so as to control the operation of the memory device since such technique is well known in the art.

With respect to claim 28, the use of a plug-in module in a memory system for the purpose of reducing the size of the system would have been obvious since such technique is well known and conventional in the memory art.

Response to Arguments

6. With respect to the applicant argument on the rejection of claims 1-58, the applicant argues that the reference of Lowrey et al fail to dislose "first and second programmable conductor memory element for storing complementary binary digit values", however such feature is shown in Lowrey et al. To be more specific, the programmable memory elements 120 and 130 (figure 2a) would store "0" and "1" that are binary digit values and one is complementary to the other ("1" is a complement to "0").

Regarding on the argument on newly added claim 59, the gate of the access transistor Q1 is inherently connected to a row address decoder that is considered as a circuit for operating access transistor. Note that every memory device must have a row decoder connected to the word line or row line (RL1) so as to select an address of a memory cell.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nam t Nguyen whose telephone number is 703-305-6494. The examiner can normally be reached on 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 703-308-2816. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

N Nguyen
May 20, 2003

Vu A. Le
Primary Examiner